REMARKS

Claims 1-17 are pending in the present application. Claims 1 and 10 are amended above. Claim 13 is canceled above. No new matter is added by the claim amendments. Entry is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

Claims 1 and 7-17 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chang (U.S. 6,125,060). Claims 2-7 are rejected as being unpatentable over Chang in view of Yi (U.S. 5,455,792) . Reconsideration and removal of these rejections are respectfully requested in view of the foregoing amendments and the following remarks.

The present invention of amended claim 1 is directed to a non-volatile semiconductor memory device. The device includes a substrate, a charge storage region on the substrate, and a control gate on the charge storage region. A gate mask is provided on the control gate, wherein the gate mask is in the shape of a spacer. The gate mask operates as an etch mask during fabrication of the semiconductor memory device to define the underlying charge storage region and the control gate.

The present invention as claimed in amended claim 1 thus includes a "gate mask" in the "shape of a spacer". As shown and described in the present specification at FIG. 7D (see page 13, line 23 - page 14, line 3), a gate mask 526' is formed by anisotropically etching the gate mask layer 526 (see FIG. 7C). In this manner, the gate mask 526' has the shape of a spacer. The spacer-shaped gate mask 526' is used first to etch the underlying layers 512, 516, 510, 514 (see FIG. 7D) in the source region 550, and later to etch the underlying layers 512, 516, 510, 514 (see FIG. 7H) opposite the source region 530 where the select gate 506 is eventually formed (see FIG.

7I). Thus, the spacer-shaped gate mask 526' is used as a mask during processing to define the underlying "charge storage region", for example comprised of floating gate dielectric 514, floating gate 510', and interpoly dielectric 516 (see FIG. 6), or comprised of the ONO charge storage layers 820 (see FIG. 9J). The spacer-shaped gate mask is also used during processing to define the underlying "control gate" 512', 812' in a similar manner.

Chang is cited in the Office Action at page 2, section 2 as disclosing, at FIG. 7d, a "gate mask 122, 125 on the control gate, wherein the gate mask is in a shape of a spacer". Close inspection of Chang reveals, however, that the spacer-shaped structure is indeed not a "etch mask" that is used to define the underlying "control gate" and "charge storage region", as claimed in amended claim 1, but instead is a structure that is later added, that is, following formation of the underlying control gate CG and floating gate 103. Particularly, the spacer structure on the control gate in Chang is a result of formation of the LDD spacer on the left side of the select gate SG (see Chang, column 9, lines 26-29). In view of this, it is submitted that the spacer structure on the control gate CG of Chang in no way serves as a "gate mask" that is used as an etch mask during fabrication to define the underlying charge storage region and control gate as claimed in claim 1.

In view of the above, it is submitted that Chang fails to anticipate the present invention as claimed in amended claim 1. Accordingly, reconsideration of the rejection and allowance of claim 1 are respectfully requested. With regard to dependent claims 2-9, it follows that these claims should inherit the allowability of the independent claim from which they depend.

The present invention of amended claim 10 is directed to a non-volatile semiconductor memory device. The device includes a substrate having a source and a drain. A channel is provided between the source and the drain. A charge storage region is provided over the channel. A control gate is provided over the charge storage region. A gate mask is formed on an entire top surface of the control gate and is in the shape of a spacer. A select gate is on the channel and

between the charge storage region and the drain. The charge storage region, the channel, the drain, the control gate and the select gate form a first unit cell.

The present invention as claimed in amended claim 10 thus includes a gate mask that is formed "on an entire top surface of the control gate". Reference is made, for example, to FIG. 6 of the present specification, which shows gate mask 526' covering an entire top surface of the control gate 512'.

It is submitted that Chang fails to teach or suggest the invention as claimed in amended claim 10. In particular, Chang fails to teach or suggest a "gate mask" that is formed "on an entire top surface of the control gate". In Chang, as explained above, the spacer-shaped structure on the control gate CG as shown in FIG. 7d, is not in any way an "etch mask", but instead is a structure that is later added, following formation of the underlying control gate CG and floating gate 103. In any event, the spacer shaped structure does not cover an "entire top surface of the control gate" as claimed in amended claim 10. Rather, the spacer-shaped structure covers only a small part of the control gate CG, leaving the control gate CG exposed to damage during subsequent processing steps.

In view of the above, it is submitted that Chang fails to anticipate the present invention as claimed in amended claim 10. Accordingly, reconsideration of the rejection and allowance of claim 10 are respectfully requested. With regard to dependent claims 11-17, it follows that these claims should inherit the allowability of the independent claim from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Claims:

Claims 1 and 10 are amended above as follows:

1. (Amended) A non-volatile semiconductor memory device comprising:

a substrate;

a charge storage region on the substrate;

a control gate on the charge storage region; and

a gate mask on the control gate, wherein the gate mask is in the shape of a spacer, the gate mask operating as an etch mask during fabrication of the semiconductor memory device to define the underlying charge storage region and the control gate.

10. (Amended) A non-volatile semiconductor memory device comprising:

a substrate having a source and a drain;

a channel between the source and the drain;

a charge storage region over [on] the channel;

a control gate over [on] the charge storage region;

a gate mask being formed on an entire top surface of the control gate and being in the shape of a spacer; and

a select gate on the channel and between the charge storage region and the drain; the charge storage region, the channel, the drain, the control gate and the select gate forming a first unit cell.